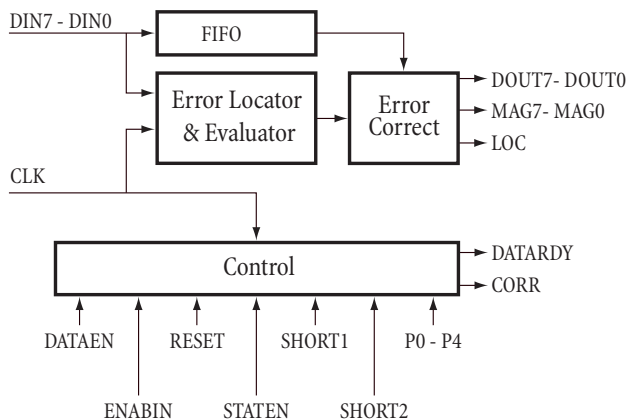


# WSC5128A Specifications

*t = 4 to 10, 320 Mbps,  
Programmable Reed-Solomon  
Forward Error Correction Decoder*



## Introduction

The WSC5128A is a modern high data rate programmable Forward Error Correction device that can decode Reed-Solomon code blocks of up to 255 eight bit data symbols. It provides corrections of up to 10 symbol errors per block at data rates up to 320 Mbps. Blocks with excessive errors are uncorrectable and are so flagged with data outputted as received ( no corrections ).

The decoder input code block will contain the transmitted data and parity symbols, as corrupted by channel noise (errors). A symbol error is corrected the same regardless of the number of incorrect bits in the symbol, and decoding time is the same regardless of the number of errors in a block. Decoder output data will be corrected data plus corrected parity or block error data. Error location and correction data is also provided.

The WSC5128A uses the primitive polynomial

$$P(x) = x^8 + x^4 + x^3 + x^2 + 1$$

which complies with SMPTE D-1 / D-2 Digital Video Standards, DVBS Digital Video, ANSI ID-1 / ID-2, and MIL STD 2179A. The WSC5128A is pin and functionally compatible with the T=5 AMPEX 1295126-01. It includes features not found in that device, and using  $t = 10$  corrects up to 10 errors per block.

The generator polynomial, dependent on the variable "r" is :

$$G(x) = \prod_{i=0}^{r-1} (x - \alpha^i)$$

Valid block lengths in AMPEX compatible mode are defined by the relationship:  $5R + 15 \leq N \leq 255$ . However, if shorter block lengths are desired just pull up the pins labeled **SHORT1** or **SHORT2** to a logic HIGH level. The valid relationship for block lengths under this condition is given in Table 2.



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### Features and Benefits (for all devices unless noted)

- Supports 8 bit symbol Reed-Solomon codes (  $N, N-r$  ) with  $8 \leq r \leq 20$  and  $N \leq 255$ .  $N$ = symbols per block including parity,  $r$  = number of parity symbols (NOTE: normally  $r = 2t$ )
- Selectable latency (  $2N + 5r + 33$  ) or (  $2N + 2r + 13$  ) or (  $3N/2 + 3r/2 + 5$  ) clock cycles and minimum code length (  $5r + 15$  ) or (  $2r + 13$  ) or (  $3r/2 + 1$  ) bytes
- Contains complete device. No external memory or control required after initialization
- Data rates up to 320 Mbps with 0 to 40 Mhz symbol clock, higher rates available
- Input and output data are always at the identical rate
- Corrects 0 to 10 errors per block
- Provides Pass Through Mode ( no correction ) switching on-the-fly
- Latency is constant regardless of error patterns
- Allows code rate change ( less data, same parity ) on-the-fly
- Provides complete error location and correction information
- Flags uncorrectable blocks
- 68-Pin PLCC
- 4.5 to 5.5 volt operation
- -40 to + 85 degrees C operation range (extended range available )
- ISO 9000 certified manufacturing

### Effectiveness of Reed-Solomon FEC

Reed-Solomon error correction codes can have an extremely pronounced effect on the efficiency of a digital communication channel. For example, an operation running at a data rate of 1 Mbps will carry approximately 4,000 blocks of 255 bytes each second. If 1,000 random short errors (less than 17 bits in length) per second are injected into the channel, about 600 to 800 blocks per second would be corrupted. By applying Reed-Solomon FEC using a 255,239 code (corrects up to 8 errors per block of 235 information bytes and 16 parity bytes), the typical time between blocks that cannot be corrected requiring retransmission, will be about 800 years. The meantime between incorrectly decoded blocks will be over 20 billion years.

### Functional Description

The device contains a decoder that will provide (  $N, N-r$  ) Reed-Solomon forward error correction decoding of blocks of eight bit symbols. The number of parity symbols (  $r$  ) may be from 0 to 20, 0 in Pass Through Mode, and the number of symbols in a block (  $N$  ) up to 255 . Two parity bytes will be used for each symbol error correction. This device will provide correction of up to 10 symbol errors (  $E$  ) as long as  $2E \leq r$ . It will provide the number of corrections made in each block. Symbol errors are processed the same regardless of the number of incorrect bits in the symbol.

The device can decode at data rates from 0 to 40 million symbols per second (320 Mbps) and two or more devices can be used together (see Application Brief for Reed-Solomon FEC) to process data at higher rates.

### Data Flow

Data enters the device via the **DIN7 - DINO** inputs on the rising edge of **CLK**. This data then takes two separate paths: path 1 into the FIFO and path 2 into the Error Locator and Evaluator.

The purpose of the FIFO is to hold the incoming message data blocks which will have error correction applied, if necessary, by the error correction circuitry before being output.

The purpose of the Error Locator and Evaluator is to generate the polynomials used to find and correct any erroneous bytes. These polynomials are then transferred to the Error Correction circuit where the error equations are solved. The error information is then shifted out in step with the corresponding data contained in the FIFO. The errors are subtracted from the original message to leave corrected data, which is output on the **DOUT7 - DOUT0** bus on the rising edge of **CLK**. The number that was subtracted appears on the **MAG7 - MAG0** bus.

The control circuitry takes care of the timing required for initialization and coordination of the various chip functions. It also generates the external timing and control signals for determining the difference between data and check bytes, as well as signaling whether the outgoing data block is correct.



### Signal Description

Table 1: Signal Description

Name	Description
ENABIN	Correction Enable. Assertive HIGH. When this input is asserted, the device performs corrections on the message block. When ENABIN is LOW the device does not perform corrections but continues to report status if initialized to do so.
DATAEN	Data Enable. Assertive HIGH. This input is used to signal the difference between data bytes and check bytes.
P4-P0	Parity Select Bus. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to # of check bytes (R). P4 is the most significant bit. P0 is always 0, so the value of P is always even.
CLK	Master Clock. All inputs and outputs are synchronized by the rising edge of CLK.
RESET	System Reset. Assertive LOW. Reset timing is critical to the initialization of the device.
STATEN	Status Enable. Assertive HIGH. If this signal is HIGH during reset then the decoder will be programmed to output two status bytes with each message block.
SHORT1 SHORT2	Latency Select. Selects latency and minimum block size, according to Table 2.
CORR	Message Block Corrected. Assertive HIGH. Indicates that errors have been found and corrected in message block.
UNCORR	Uncorrectable Block. Assertive HIGH. Indicates message block contains uncorrectable errors.
DATARDY	Data Ready. Assertive HIGH. This output is held HIGH for data bytes and low for check bytes.
DIN 7-0	Data input bus. Bit 7 is the most significant.
DOUT 7-0	Data output bus. Bit 7 is the most significant.
LOC	Error Location. Assertive HIGH. This output goes HIGH if the current symbol output on DOUT7 - DOUT0 has had a correction applied to it.
MAG 7-0	Error Magnitude. These outputs indicate which bits of the current symbol output on DOUT7 - DOUT0 has been corrected when LOC is HIGH. These outputs are indeterminate and should be ignored when LOC is LOW.

### Latency Description

Table 2: Latency and Minimum Block Size Selection

SHORT1	SHORT2	Latency	Minimum Block Size
0	0	$2N + 10t + 33$	$10t + 15$
1	0	$2N + 4t + 13$	$4t + 13$
0	1	$3N/2 + 3t + 5$	$3t + 1$
1	1	$3N/2 + 3t + 5$	$3t + 1$



## Correction Parameters

Table 3: Parameter Definition

Name	Description
R	The total number of check bytes used for both detection and correction. Since this device is programmable, R may vary from 8 to 20. It takes two check bytes to correct each error.
N	The total number of bytes in one message block including data and check bytes. This number must be at least $5R + 15$ in AMPEX compatible mode, at least $2R + 13$ in non-compatible mode, or $3R/2 + 1$ in shortest latency mode. This number must be no greater than 255.
K	The number of data bytes in one message block ( $K = N - R$ )
P	The threshold for determining uncorrectability of a data block, and the number of check bytes allocated for correction only purposes (and not for detection). When the number of errors exceeds the threshold set by P, then the block is flagged uncorrectable, the CORR pin goes LOW, and no corrections are performed.
E	The number of errors in a received message block. An error is defined as an erroneous byte whose correct value and position within the message block are both unknown.

## Basic Operation

The W5C5128A is a very flexible device. It was specifically designed to be a replacement for the AMPEX 1295126-001. However, it is capable of operating at a lower latency and on smaller minimum block sizes than the AMPEX part and is capable of correcting up to a maximum of 10 errors. The AMPEX part can only correct 5. The W5C5128A will also output error location and pattern information. The AMPEX part doesn't have this capability. The AMPEX part is rated at 15 MHz whereas the W5C5128A is rated at 40 MHz.

## Initialization

Certain architectural and mathematical properties of this device are not hard wired and must be set up during the initialization control sequence. These properties include:

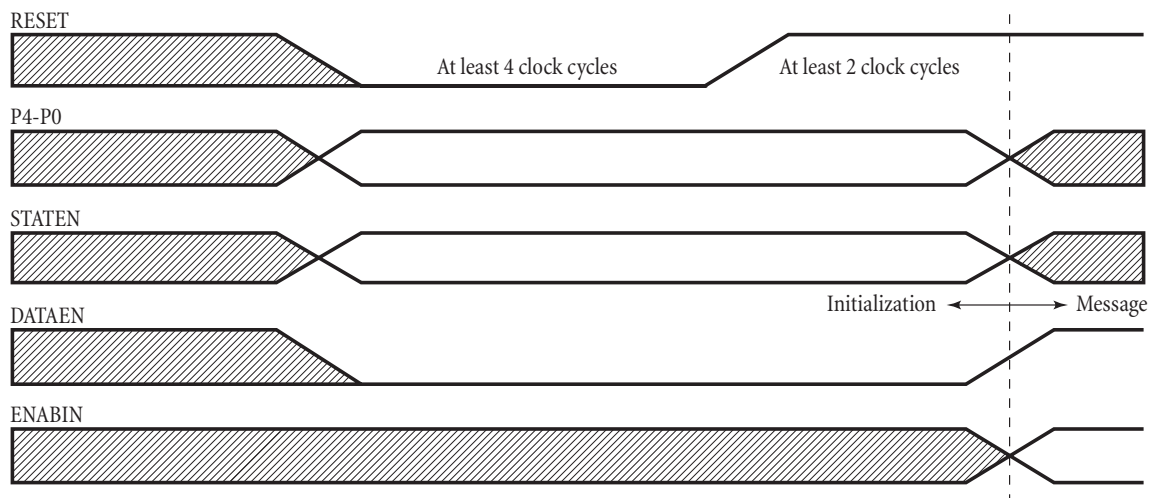
1. The overall message block length (N)
2. The number of data bytes (K)
3. The total number of check bytes (R)
4. The number of check bytes allocated for correction only (P)
5. Whether the first check byte output positions are used for status bytes or check bytes (STATEN)
6. Whether to use AMPEX compatible, non-compatible, or short timing (SHORT1, SHORT2)

These properties must be initialized before normal operation can begin. There are two distinct phases of the initialization process. In phase one, the values of P, STATEN and SHORT1 and SHORT2 are initialized. In phase two, the first message block through the device is used to set the values of N, K and R.



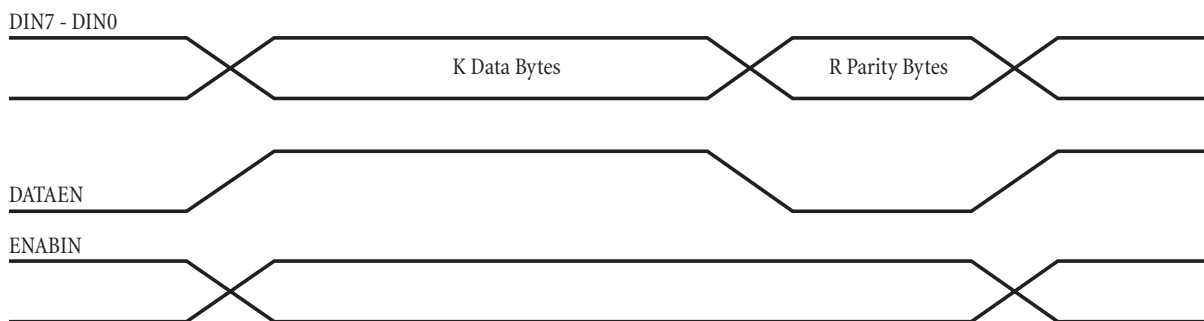
The phase one sequence consists of at least 4 clock cycles in which **RESET** is held LOW followed by at least 2 clock cycles during which **RESET** is held HIGH. **RESET** must then remain HIGH for all subsequent operations or else an unwanted initialization sequence will ensue. The desired values of **STATEN** and **P4 - P0** must be maintained during the first phase of initialization. The desired value of **SHORT1** and **SHORT2** must be maintained during all the phases of operation of the device. **DATAEN** must be held LOW during the entire six clock sequence or unintended processing of spurious messages may occur.

Figure 4a Initialization Control Sequence Timing



The rising edge of **DATAEN** at the end of the phase one initialization sequence marks the beginning of the first message block, which is the beginning of phase two of the initialization process. **DATAEN** has the role of initializing the parameters of N, K and R. **DATAEN** has a different function on all subsequent blocks until an initialization sequence is begun once again. As the first message block passes through the device, **DATAEN** is held HIGH for K clock cycles and then LOW for R clock cycles. **DATAEN** going high again marks the first byte of the second block and implies the end of the phase two initialization sequence. **DATAEN** has thus defined R, K and N for all subsequent blocks until another initialization sequence is performed.

Figure 4b Message Input Timing



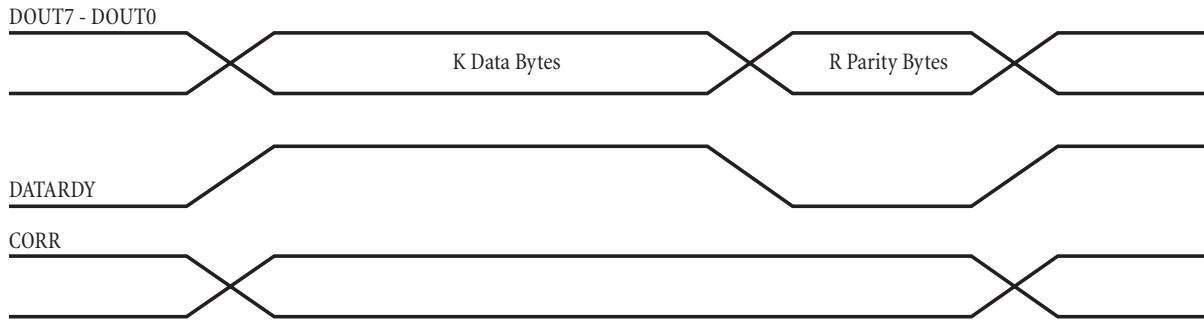
**Message Decoding**

During message decoding the device clocks in the encoded message block from the **DIN7 - DIN0** input bus on the rising edge of **CLK**. The device then computes polynomials for this data using a high performance Reed-Solomon coding algorithm, and then proceeds to use the



calculated polynomials to correct any errors, if possible. These polynomials are a series of complex equations that will indicate not only the position of incorrect bytes but will also produce the necessary information to correct them. The timing of the decoding operation is defined in figure 4b for the input and in 4c for the output.

**Figure 4c Message Output Timing**



The action taken by the decoder with respect to a given message block is determined in all cases by the quantity of errors received. The device reports its action via the **CORR** output pin. If  $P = R$ , a HIGH output on the **CORR** pin indicates that the message block being output is correct. A LOW output indicates that a correction was not performed because there were too many errors or no errors. In situations where  $P$  has been chosen to be not equal to  $R$ , the meaning of the **UNCORR** pin is that more than  $P/2$  errors have occurred.

#### **Optional Status Bytes**

The optional status bytes, that may be output at the end of the message block, indicate the number of errors encountered and may be used to determine the exact meaning of the **CORR** output when  $P \neq R$ . The first status byte has all of its bits set LOW except bit 7, which is the CA (correction attempted) flag. The CA flag goes LOW when  $E \leq R/2$  (the message block was successfully decoded). Therefore, anytime CA is HIGH, the message block should be retransmitted since there were probably too many errors to reliably correct. Also, if  $P = R$  then CA will always be LOW when the **CORR** output pin is HIGH and HIGH when **CORR** is LOW.

In the second status byte, bits 4 through 0 are a binary count of the number of errors encountered. Bit 4 is most significant. The remaining bits are always LOW.



## Pinout

Table 4: Device Pinout

Pin#	Name	Function	Type
1	DATAEN	Data Enable	I
2	ENABIN	Correction Enable	I
3	V <sub>dd</sub>	+ 5V Power	P
4	P3	Parity Select Bus	I
5	P2	Parity Select Bus	I
6	P1	Parity Select Bus	I
7	P4	Parity Select Bus, MSB	I
8	N / C **	No Connect	
9	SHORT1	Latency Select 1	I
10	N / C **	No Connect	
11	N / C **	No Connect	
12	RESET	Reset	I
13	V <sub>dd</sub>	+ 5V Power	P
14	V <sub>ss</sub>	Ground	P
15	Test_S0	No Connect	
16	SHORT2	Latency Select 2	I
17	V <sub>ss</sub>	Ground	P
18	N / C**	No Connect	
19	N / C**	No Connect	
20	CLK	Device Master Clock	I
21	CORR	Message Block Correct	O
22	EOB	End of Block	O
23	DOUT7	Data output bus, MSB	O
24	LOC	Error location flag	O

Table 4: Device Pinout continued

Pin#	Name	Function	Type
25	V <sub>ss</sub>	Ground	P
26	V <sub>dd</sub>	+ 5V Power	P
27	MAG0	Error Magnitude Bus, LSB	O
28	MAG1	Error Magnitude Bus	O
29	MAG2	Error Magnitude Bus	O
30	DOUT6	Data Output Bus	O
31	DOUT5	Data Output Bus	O
32	V <sub>ss</sub>	Ground	P
33	DOUT4	Data Output Bus	O
34	DOUT3	Data Output Bus	O
35	V <sub>dd</sub>	+ 5V Power	P
36	DOUT2	Data Output Bus	O
37	DOUT1	Data Output Bus	O
38	V <sub>ss</sub>	Ground	P
39	DOUT0	Data Output Bus, LSB	O
40	DATARDY	Data Ready	O
41	MAG3	Error Magnitude Bus	O
42	MAG4	Error Magnitude Bus	O
43	MAG5	Error Magnitude Bus	O
44	V <sub>dd</sub>	+ 5V Power	P
45	V <sub>ss</sub>	Ground	P
46	MAG6	Error Magnitude Bus	O
47	STATEN	Status Enable	I
48	MAG7	Error Magnitude Bus, MSB	O

Note \*\*: No Connection pins do not have to be tied down with an external resistor.  
 I = Input ; O = Output ; P = Power

Table 4: Device Pinout *continued*

Pin#	Name	Function	Type
49	DIN7	Data Input Bus, MSB	I
50	N / C**	No connection	
51	DIN6	Data Input Bus	I
52	N / C**	No Connect	
53	V <sub>dd</sub>	+ 5V Power	P
54	TEST_SI	No Connect	
55	DIN5	Data Input Bus	I
56	V <sub>ss</sub>	Ground	P
57	V <sub>dd</sub>	+ 5V Power	P
58	DIN4	Data Input Bus	I

Table 4: Device Pinout *continued*

Pin#	Name	Function	Type
59	DIN3	Data Input Bus	I
60	N / C**	No Connect	
61	UNCORR	Message Block Uncorrectable	O
62	N / C**	No Connect	
63	N / C**	No Connect	
64	DIN2	Data Input Bus	I
65	DIN1	Data Input Bus, LSB	I
66	V <sub>dd</sub>	+ 5V Power	P
67	DIN0	Data Input Bus, LSB	I
68	V <sub>ss</sub>	Ground	P

Note \*\*: No Connection pins do not have to be tied down with an external resistor.

I = Input ; O = Output ; P = Power

### Electrical Specifications

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V <sub>dd</sub>	Supply Voltage	-0.3	6.0	V
V <sub>i</sub>	Voltage at Digital Inputs	-0.3	V <sub>dd</sub> + 0.3	V
V <sub>o</sub>	Voltage at Digital Outputs	-0.3	V <sub>dd</sub> + 0.3	V
T <sub>stg</sub>	Storage Temperature	-65	+150	°C
I <sub>i</sub>	Current into Digital Inputs	-10.0	+10.0	mA
I <sub>o</sub>	Current into Digital Outputs	-10.0	+10.0	mA



Table 6: Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{dd}$	Supply Voltage	4.5	5.5	V	
$T_{op}$	Operating Temperature	- 40	+ 85	°C	Commercial Grade
$V_i$	Voltage at Digital Inputs	0	$V_{dd}$	V	
$I_{dd}$	Supply Current		100	mA	

Table 7: DC Electrical Characteristics

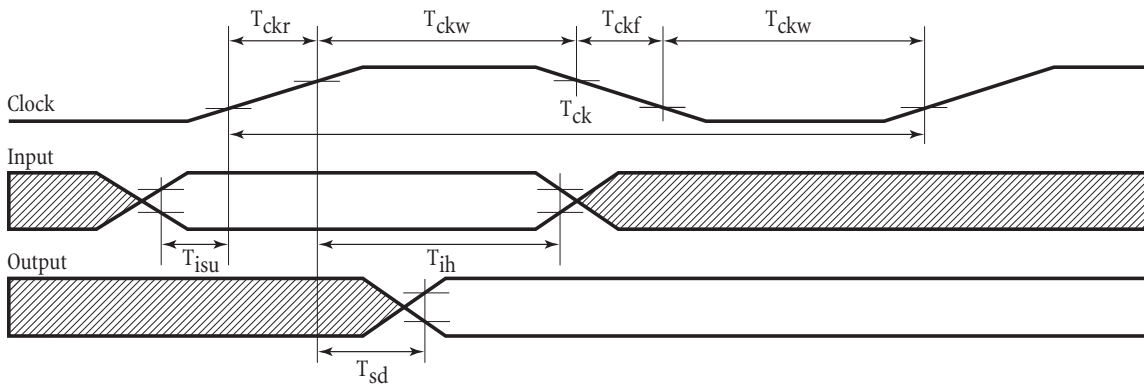
Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{il}$	Input Low Voltage		0.8	V	
$V_{ih}$	Input High Voltage	2.2		V	
$V_{ol}$	Output Low Voltage		0.4	V	$I_{ol} = 4.0 \text{ mA}$
$V_{oh}$	Output High Voltage	3.5		V	$I_{oh} = + 4.0 \text{ mA}$
$I_{il}$	Input Leakage	-1	+1	$\mu\text{A}$	$V_{ih} = V_{dd}, V_{il} = V_{ss}$ No pull up or down
$R_i$	Input Resistance				50 K $\Omega$ typical
$I_{dds}$	Static Current		100	$\mu\text{A}$	$V_{in} = V_{dd}$ or $V_{ss}$ $I_{oh} = I_{ol} = 0$
$C_{in}$	Input Capacitance				3 pF typical
$C_{out}$	Output Capacitance				3 - 6 pF typical



Table 8: AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units	Test Conditions
$T_{ck}$	Clock Cycle Time	40		ns	Valid $V_{il}$ to valid $V_{il}$
$T_{ckr}$	Clock Rise Time		6	ns	Valid $V_{il}$ to valid $V_{ih}$
$T_{ckf}$	Clock Fall Time		6	ns	Valid $V_{ih}$ to valid $V_{il}$
$T_{ckw}$	Clock Pulse Width	15		ns	Valid $V_{il}$ to valid $V_{il}$ or Valid $V_{ih}$ to valid $V_{ih}$
$T_{isu}$	Data / Control Input Set-up	5		ns	Valid $V_{il}$ or $V_{ih}$ to invalid $V_{il}$
$T_{ih}$	Data / Control Input Hold	0		ns	Valid $V_{ih}$ to invalid $V_{il}$ or $V_{ih}$
$T_{sd}$	Data / Control Output Delay		15	ns	$C_l = 50$ pF

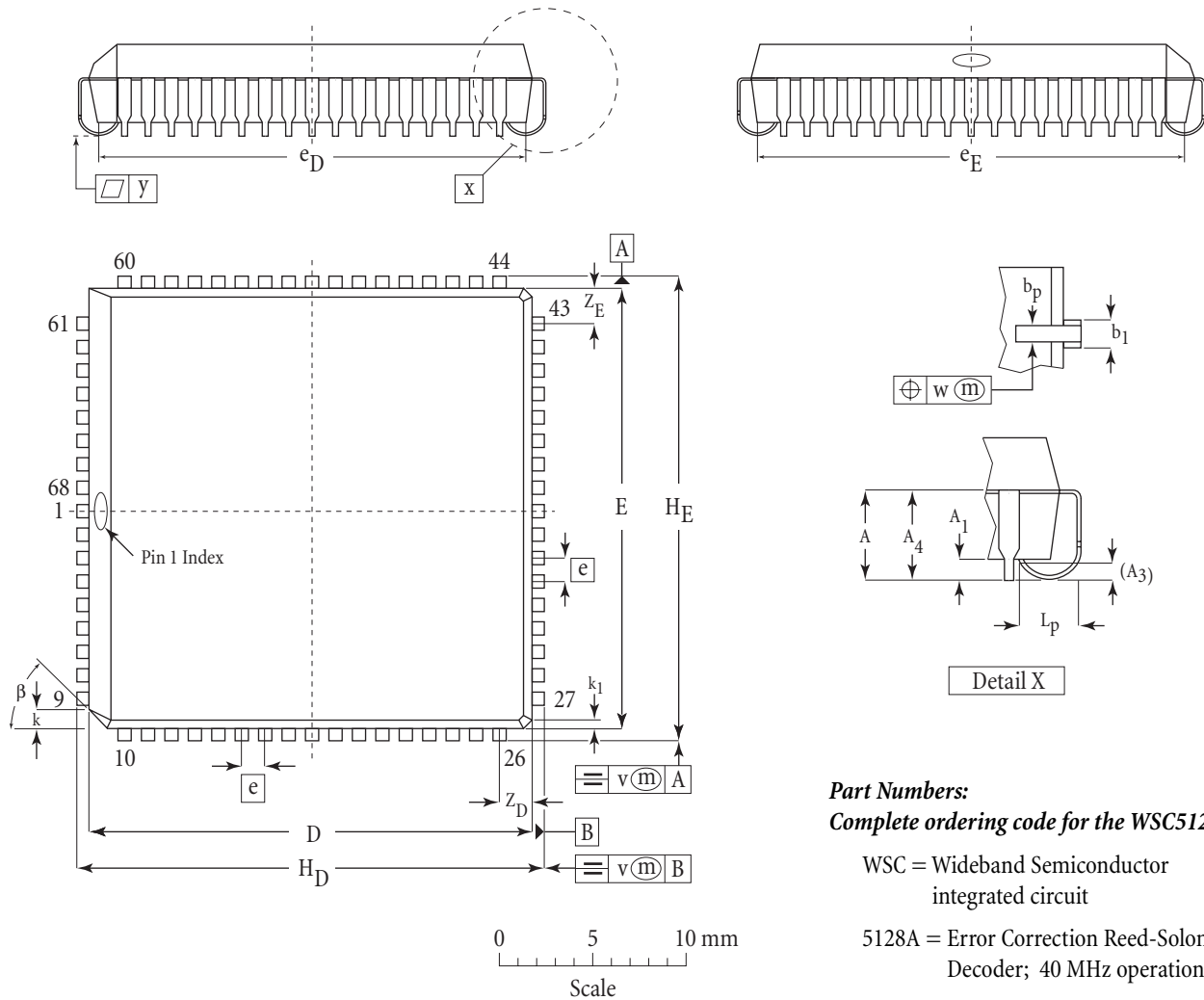
**Output Timing**





7.0 Packaging

Table 9: PLCC Dimensions



**Part Numbers:**

**Complete ordering code for the WSC5128A**

WSC = Wideband Semiconductor  
integrated circuit

5128A = Error Correction Reed-Solomon  
Decoder; 40 MHz operation

PJ = plastic j leaded chip carrier

I = -40 to + 85 °C operating temperature range

Parts are packaged in anti-static tubes of  
20 units each

Unit	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D	E	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	k <sub>1</sub> max.	L <sub>p</sub>	v	w	y	Z <sub>D</sub> max.	Z <sub>E</sub> max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

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