

WCI8130A Specifications

Reed-Solomon Evaluation Board

User Manual

Up to 40 Msymb/sec



Board Specification

Features

- COic5127A Reed-Solomon Encoder
- COic5128A Reed-Solomon Decoder
- Block Lengths up to 255 bytes
- T=4 to 10
- Programmable Test Patterns
- Programmable Error Patterns
- Host Interface to PC for Operation
- -40 C to + 85 C operation
- Available now
- Version available for COic5130A upon request
- Schematics included
- Source software included



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1.0 Introduction

The WCI 5127A/5128A Reed-Solomon evaluation board allows the user to evaluate the performance of the COic 5127A Reed-Solomon encoder and the COic 5128A Reed-Solomon decoder. In addition a complete reference design for incorporation into production system is provided including schematics. Software is provided to setup various test scenarios validate error and error checking performance.

1.1 Key Features

The WCI 5127A/5128A Reed-Solomon evaluation board provides the following key features:

- Supports T=4 to T=10 operation
- Supports codeword lengths up to 255 bytes.
- Uncorrectable errors are flagged
- Error magnitudes are available
- Operation up to 40 MHz

1.2 Applications

- Digital TV transmission systems
- Digital cable hubs
- High performance cable modems
- LOS microwave radio
- Wireless LAN
- Wireless ATM

1.3 Block Diagram

A block diagram of the evaluation board architecture is shown in Figure 1.

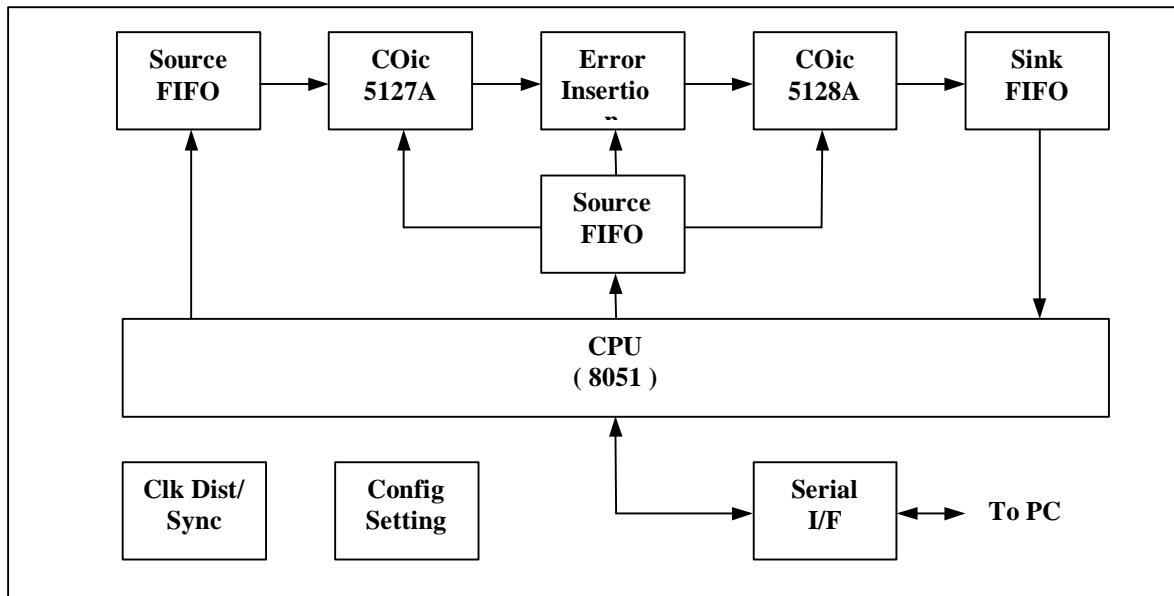


Figure 1
Reed-Solomon Evaluation Board Architecture

2.0 Functional Overview

The WCI 5127A/5128A Reed-Solomon evaluation board allows the user to define a source vector test set to play through the encoder, an error vector set to introduce errors into the simulated channel, and to view the resultant data at the output of the decoder. The evaluation board is controlled by an 8051 microcontroller that coordinates the test scenarios, downloads test vectors from a PC, and uploads results to the PC.

The evaluation board consists of the following components:

- CPU (CPU.SCH)
- Serial Interface (SERIAL.SCH)
- Configuration Settings (CONFIG.SCH)
- Clock Distribution (CLOCK.SCH)
- Source Data FIFO (SOURCE.SCH)
- Control Data FIFO (CTRL.SCH)
- Reed-Solomon Encoder (RSENC.SCH)
- Error Insertion Logic (ERROR.SCH)
- Reed-Solomon Decoder (RSDEC.SCH)
- Output Data FIFO (SINK.SCH)
- Synchronizer Logic (SYNC.SCH)
- Power and Pullups (PWR.SCH)

2.1 CPU

The WCI 5127A/5128A Reed-Solomom evaluation board is controlled by a 8051 microcontroller (U8). The microcontroller coordinates the downloads from the PC for various test scenarios, loads the source data and control data fifos, and uploads the received codewords from the output data fifo. The CPU synchronizes the data input to the Reed-Solomon encoder with the crystal controlled clock.

2.2 Serial Interface

The serial interface is configured for RS-232 operation at 1200 baud with a PC. The serial interface is implemented by an RS-232 converter (U10) and Port 3 of the 8051 CPU (U8). A cable is provided. Tantalum capacitors (C4, C5, C6, C7 and C8) are provided as part of the charge pump circuit for the RS-232 converter. One bypass capacitor (C30) is provided.

2.3 Configuration Settings

The length of T (maximum number of corrections) for the encoder and the length of P (number of parity bytes) for the decoder are set by jumpers in the configuration circuit. A jumper inserted is equivalent to a "0" logic level at the pin on the encoder or decoder. The following is a table for the T jumpers.

Encoder	PinJumper
TA3 (pin 9)	JP1-3 (0=Jumper Inserted/1=Jumper Removed)
TA2 (pin 3)	JP1-2 (0=Jumper Inserted/1=Jumper Removed)
TA1 (pin 4)	JP1-1 (0=Jumper Inserted/1=Jumper Removed)
TA0 (pin 5)	JP1-0 (0=Jumper Inserted/1=Jumper Removed)

The following is a table for the P jumpers.

Decoder Pin	Jumper
P4 (Pin 7)	JP2-4 (0=Jumper Inserted/1=Jumper Removed)
P3 (pin 4)	JP2-3 (0=Jumper Inserted/1=Jumper Removed)
P2 (pin 5)	JP2-2 (0=Jumper Inserted/1=Jumper Removed)
P1 (pin 6)	JP2-1 (0=Jumper Inserted/1=Jumper Removed)
P0 (pin 11)	Always a "0"



2.4 Clock Distribution

Since the WCI 5127A and WCI 5128A devices are hi-speed synchronous logic it is important to maintain the proper setup and hold times. To minimize clock skew, a some form of clock distribution is recommended. The output of the TTL oscillator (U12) is connected to the input of a low skew clock distribution chip (U11). All outputs from this chip have a guaranteed skew of less than 250 ps. Note that since the propagation times for inputs to the WCI 5127A and WCI 5128A are typically 6 to 10 ns, clock skew is not particularly critical. However, proper clock waveforms at the destination devices is achieved through serial termination of the individual clocks. Bypass capacitors (C31 and C32) are used for TTL oscillator and clock distribution chip.

2.5 Source Data Fifo

The source data FIFO (U1) stores up to 4096 test vectors downloaded from the PC. The test vectors within this fifo are the first 16 bits of each record in the download test. The format for the downloaded record is provided in section 3.1. The first 16 bits are the message and error vectors.

2.6 Control Data Fifo

The control data FIFO (U2) stores up to 4096 control test vectors from the PC. The control test vectors set the control pins for the Reed-Solomon encoder and decoder for each clock cycle. These include ENINA, ENOUTA and RESET for the encoder, and SSET, CEN, DEN, SHORT1, SHORT2, and RESET for the decoder. The format within the download record is discussed in section 3.1.

2.7 Reed-Solomon Encoder

The Reed-Solomon encoder (U3) accepts message bytes from the Source fifo, control data from the Control fifo, and configuration data (length of T) from the configuration circuit. Operation of the Reed-Solomon encoder is fully described in the COic 5127A data sheet.

2.8 Error Insertion Logic

The error insertion logic allows the user to test the ability of the decoder to correct errors. Two PALs (U4 and U5) accept error patterns from the source data FIFO and XOR these errors into the codeword stream.

2.9 Reed Solomon Decoder

The Reed-Solomon decoder (U6) accepts codeword bytes from the output of the error insertion logic and outputs corrected codewords to the output data FIFO. In instances where the number of errors exceeds the error correction capability, an uncorrectable error will be indicated.



2.10 Output Data Fifo

The output data FIFO (U7) stores the output of the decoder so that it may be compared to the original message to verify error correction capability. The data stored within the output data FIFO may be uploaded to the PC for comparison.

2.11 Synchronizer Logic

The test vectors stored in the source data control data FIFOs are output upon command from the CPU. The data must be synchronized and this function is provided by another PAL (U13). This is not a problem in a typical synchronous modem design. This is simply required by the evaluation board.

2.12 Power and Pullups

The power required is +5V at 3A maximum. One of the CPU's ports requires pullups and several test points are provided.

3.0 User Interface

The user interface provide the capability to download files and upload files. Sample files for various block lengths and values of T are provided.

3.1 Download File Record Format

Each record downloaded to the Reed-Solomon evaluation board must have the following hex format:

AA BB C DD,

Where,

AA : 8-bit Message or Blank Parity Byte
BB : 8-bit Error Byte (or 0 for no errors inserted in this byte)
C : 3-bit control for Encoder
Bit 2 = ENINA
Bit 1 = ENOUTA
Bit 0 = RESET



DD : 5-bit control for Decoder
Bit 4 = SSET
Bit 3 = CEN
Bit 2 = DEN
Bit 1 = SHORT2
Bit 0 = SHORT1

3.2 Upload File Record Format

Each record uploaded from the Reed-Solomon evaluation board will have the following hex format:

EE FF,

Where,

EE : 8-bit Received Codeword byte
FF : 8-bit Error Magnitude byte

4.0 Schematics

The schematics are available for download as PDF files. The top level schematic is Cooptic.pdf.